REMARKS

I. Status of Claims

Claims 1-8 are pending in this application. Claims 1 and 3 are independent.

Claims 1-8 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement.

Claims 1-8 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Fujita Yoshihiro (05-053898) (hereinafter "Fujita") in view of Kobayashi et al (USP 4,550,437) (hereinafter "Kobayashi").

The Applicant respectfully request reconsideration of these rejections in view of the following remarks.

II. 35 U.S.C. § 112, first paragraph, Rejection

The Examiner states that the previous amendments raise new matter issues. Accordingly, in the following chart and remarks, the Applicant respectfully submits how the previous amendments are based on the specification and drawings.

Claim 1	Relevant Portions of Specification
1. An image processing device to multiply a two-dimensional pixel data by a matrix of coefficients and filter said pixel data based on a sum of the multiplied results, said image processing device comprising:	
a memory unit array in which a plurality of memory units in a form of matrix are arranged which at least includes a first memory cell to store said pixel data, a second memory cell and a third memory cell;	A "memory unit array" described in claim 1 corresponds to a "memory unit array 100." A "memory unit" described in claim 1 corresponds to, for example, a "memory unit 10" in Fig. 1. As shown in Fig. 1, the memory unit array 100 is comprised of a plurality of the memory units 10 arranged in a form of matrix. As in Fig. 3, one memory unit 10 includes "a first memory cell 1," "a second memory cell 2" and "a third memory cell 3" described in claim 1, and a fourth memory cell 4;
a first calculator arranged in rows of, and in the number of columns of, said memory unit array to perform computation using the pixel data stored in said first memory cell in the memory units of a same column and in a plurality of rows in the memory unit array and obtain a first processing data to store in said second	A "first calculator" described in claim 1 arranged in rows of, and in the number of columns of, the memory unit array corresponds to a "row computing section 40" in Fig. 1; and

memory cell in one memory unit among the memory units of the same column and in the plurality of rows; and	
a second calculator arranged in columns of, and in the number of rows of, the memory unit array to perform computation using the first processing data stored in said second memory cell in the memory units of a same row and in a plurality of columns in the memory unit array and obtain a second processing data to store in said third memory cell in one memory unit among the memory units of the same row and in the plurality of columns; and wherein said filtering is performed based on a computed result by the second calculator.	A "second calculator" described in claim 1 arranged in columns of, and in the number of rows of, the memory unit array corresponds to a "column computing section 50" in Fig. 1.

Further, the Applicant submits the following explanations as to the Office Action's allegations of new matter.

First, with reference to Fig. 3, the processing of the "row computing section 40" corresponding to the "first calculator" described in claim 1 is explained. In Fig. 3, as one example of memory units 10 in a plurality of rows and in a plurality of columns, 3 rows x 3 columns, of memory units 10 are shown. Here, with reference to the "row computing section 40," shown in Fig. 3, a column bus 5 is connected. This column bus 5 is connected to memory units 10 of a same column (i.e., the center column) and in a plurality of rows (i.e., upper, middle, and lower rows) among the 3 row x 3 column memory units 10 in a plurality of rows and in a plurality of columns. More specifically, the column bus 5 shown in Fig. 3 is connected to the "first memory cell 1" in the memory unit 10 of a same column (i.e., the center column) and in a plurality of rows (i.e., upper, middle, lower rows).

Next, regarding the "row computing section 40," as is described in the specification (*See* page 7, lines 14-17), the pixel data stored in the first memory cells 1 are added up as electric current value through the column bus 5 and inputted to the row computing section 40. That is, the pixel data stored in three "first memory cells 1" in the memory units 10 of a same column (i.e., the center column) and in a plurality of rows (i.e., upper, middle, and lower rows) connected to the column bus 5 are inputted to the "row computing section 40."

In the "row computing section 40," as is described in the specification (*See* page 7, lines 17-21), a computed result—obtained by trisecting the total value of the three pixel data in the first memory cells 1—is stored in the second memory cell 2 in the memory units 10 in the middle row. More specifically, as indicated by an "arrow" in Fig. 3, the "row computing section 40"

stores the computed result in the "second memory cell 2" of one memory unit 10 (in the center row in Fig. 3) among the memory units 10 in a same column (i.e., the center column) and in a plurality of rows (i.e., upper, middle, and lower rows) connected to the column bus 5. Here, the computed result stored in the second memory cell 2 corresponds to a "first processing data" described in claim 1.

In this way, in the "row computing section 40" corresponding to the "first calculator" described in claim 1, the pixel data stored in the first memory cells in the memory units 10 of a same column and in a plurality of rows is used to perform computation, and the first processing data is obtained which is stored in the second memory cell 2 of one memory unit among the memory units of the same column and in the plurality of rows.

Turning to Fig. 3, the processing of the "column computing section 50" corresponding to the "second calculator" described in claim 1 will now be explained.

Here, a row bus 6 is connected to the "column computing section 50" as shown in Fig. 3. This row bus 6 is connected to memory units 10 of a same row (i.e., the center row) and in a plurality of columns (i.e., left, middle, and right columns) among the 3 row x 3 column memory units 10 in a plurality of rows and in a plurality of columns. More specifically, the row bus 6 shown in Fig. 3 is connected to the "second memory cell 2" in the memory units 10 of a same row (i.e., the center row) and in a plurality of columns (i.e., left, middle, and right columns).

Regarding the "column computing section 50," as is described in the specification (*See* page 8, lines 4-9), the first processing data stored in the second memory cell 2 are added up as electric current value through the row bus 6, and inputted to the column computing section 50. That is, the first processing data stored in three "second memory cells 2" in the memory units 10 of a same row (i.e., the center row) and in a plurality of columns (i.e., left, middle, and right columns) connected to the row bus 6 are inputted to the "column computing section 50."

In the "row computing section 50," as described in the specification (*See* page 8, lines 9-14), a computed result obtained by trisecting the total value of the three first processing data of the second memory cells 2 is stored in the third memory cell 3 in the memory units 10 in the center column. More specifically, as indicated by an "arrow" in Fig. 3, the "column computing section 50" stores the computed result in the "third memory cell 3" of one memory unit 10 (in the center column in Fig. 3) among the memory units 10 in a same row (i.e., the center row) and

in a plurality of columns (i.e., left, middle, and right columns) connected to the row bus 6. Here, the computed result stored in the third memory cell 3 corresponds to a "second processing data" described in claim 1.

In this way, in the "column computing section 50" corresponding to the "second calculator" described in claim 1, the first processing data stored in the second memory cells 2 in the memory units 10 of a same row and in a plurality of columns is used to perform computation, and the second processing data is obtained which is stored in the third memory cell 3 of one memory unit among the memory units of the same row and in the plurality of columns.

The Applicant respectfully submits that the foregoing remarks regarding claim 1 also apply to claim 3, which is an independent method claim.

In view of the foregoing chart and remarks, the Applicant respectfully submits that no new matter was added in the previous amendment and that the Applicant respectfully requests withdrawal of the 35 U.S.C. § 112, first paragraph, rejection based on new matter.

III. Pending Claims

Independent claims 1 and 3, the only independent claims, stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Fujita in view of Kobayashi.

As shown in FIG. 1, certain embodiments of the present application concern a plurality of memory units 10 in the form of a matrix arranged in a memory unit array 100. A row computing section 40, equivalent to a first calculator, is arranged in row of, and in the number of columns of, the memory unit array 100. A column computing section 50, equivalent to a second calculator, is arranged in column of, and in the number of rows of, the memory unit array 100. In addition, as seen in Fig. 3, a first memory cell 1, a second memory cell 2 and a third memory cell 3 are provided in each of the memory unit 10.

Moreover, in certain embodiments of the present application, as seen in Fig. 3 (See also page 7, lines 14-21 of the specification), the row computing section 40, equivalent to the first calculator of Applicant's claim 1, performs computation using pixel data stored in the first memory cell 1 in the memory units 10 of the same column and in a plurality of rows (e.g., in the example of Fig. 3, three rows of the second column). A computed result (*See* e.g., "first processing data" as described on page 6, line 10, of the specification) is stored in the second

memory cell 2 in one memory unit among the memory units 10 of the same column and in the plurality of rows (e.g., in the example of Fig. 3, in a middle row among three rows of the second column).

In addition, in the present application, as seen in Fig. 3 (*See also* page 8, lines 4-14 of the specification), the column computing section 50, equivalent to the second calculator of Applicant's claim 1, performs computation using the first processing data stored in the second memory cell 2 in the memory units 10 of the same row and in a plurality of columns (e.g., in Fig. 3, three columns of the second row). A computed result (*See* e.g., "second processing data" in page 6, line 12) is stored in the third memory cell 3 in one memory unit among the memory units 10 of the same row and in the plurality of columns (in the example of Fig. 3, in a middle column among three columns of the second row).

That is, in the present application, as described in lines 8-14 on page 6 of the specification, the pixel data is stored in the first memory cell 1 in one memory unit 10, the first processing data is stored in the second memory cell 2, and the second processing data is stored in the third memory cell 3. Therefore, at least three independent data are stored in one memory unit 10.

The Office Action alleges that, in Fujita, Applicant's memory unit array recited in claim 1 is equivalent to an orthogonal memory cell 101 in Fig. 10 of Fujita, and memory units in Applicant's claim 1 is equivalent to 2x2 blocks in Fig. 10 of Fujita (namely, 1 word consisted of 2 bit x 2 bit shown as 1-4). The Office Action further alleges that a first memory cell in Applicant's claim 1 is equivalent to 2x2 block 1 in Fig. 10 of Fujita, a second memory cell in Applicant's claim 1 is equivalent to 2x2 block 2 in Fig. 10 of Fujita, and a third memory cell in Applicant's claim 1 is equivalent to 2x2 block 3 in Fig. 10 of Fujita.

In contrast to the present invention as claimed by the Applicant, in Fujita, as described in paragraph [0022], the 2x2 blocks in Fig. 10 of Fujita--which the Office Action alleges are equivalent to the memory units in Applicant's claim 1--are structured as 1 word consisted of 2 bit x 2 bit shown as 1-4. That is, in Fujita, the 2x2 blocks in Fig. 10, which the Office Action alleges are equivalent to the memory units in Applicant's claim 1, are structured as 1 word so that it can store only one processing data.

More specifically, in Fujita, as described in paragraph [0023], when data (1-4) on a row

memory 102 shown in Fig. 10 is transferred to the orthogonal memory cell 101 equivalent to the memory unit array, the data (1-4) on the row memory 102 is stored in all of 2x2 blocks (1-4) in the orthogonal memory cell 101. That is, in this case, the 2x2 blocks equivalent to the memory units in claim 1 can store the data on the row memory 102 only.

In addition, the Applicant respectfully submits that claim 3 requires "a first step to obtain a first processing data by performing computation using a pixel data stored in a first memory cell in memory units of a same column and in a plurality of rows, and store the first processing data in a second memory cell in one memory unit among the memory units of the same column and in the plurality of rows," and "a second step to obtain a second processing data by performing computation using the first processing data stored in the second memory cell in the memory units of a same row and in a plurality of columns, and store the second processing data in a third memory cell in one memory unit among the memory units of the same row and in the plurality of columns."

In contrast, in Fujita, as described in paragraph [0025], when data on a column memory 103 shown in Fig. 10 is transferred to the orthogonal memory cell 101, equivalent to the memory unit array, only the data on the column memory 103 is stored.

As described above, in the present application, at least three independent data are stored in one memory unit 10. To the contrary, in Fujita, only one data is stored. Therefore, the Applicant respectfully submits that certain embodiments of the present application as claimed by Applicant and Fujita are different. Still further, the Applicant respectfully submits that neither Kobayashi nor any of the other cited references cure the deficiencies of Fujita.

Because the present application has the above structure, in performing computation using a matrix of coefficients, it is not necessary to read out the same pixel data over and over. So, very efficient computation may be performed.

In contrast, in Fujita, when data in an orthogonal memory cell is processed at a row computing element 15 equivalent to the first calculator in Applicant's claims, the data in the orthogonal memory cell should be transferred via a row transfer circuit 17 one by one. Likewise, in Fujita, when the data in the orthogonal memory cell is processed at a column computing element 21 equivalent to the second calculator in Applicant's claims, the data in the orthogonal memory cell should be transferred via a column transfer circuit 23 one by one. Therefore, in

Fujita, in performing computation using a matrix of coefficients, the data in the orthogonal memory cell should be transferred to the row computing element 15 or the column computing element 21 one by one. This requires reading out the same pixel data over and over. So, the computation becomes very inefficient.

The present application has the above-mentioned structure to avoid reading out the same pixel data over and over. Based on this distinction, the present application and Fujita are different, and the Applicant respectfully submits that none of the cited references cure the deficiencies of Fujita.

Therefore, the Applicant respectfully submits that claims 1 and 3, as well as their dependent claims, are patentable over the cited references.

IV. Conclusion

In light of the above discussion, Applicants respectfully submit that the present application is in all aspects in allowable condition, and earnestly solicits favorable reconsideration and early issuance of a Notice of Allowance.

The Office Action is invited to contact the undersigned at (202) 220-4420 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

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